JEDEC STANDARD

Procedure for the Wafer-Level Testing of Thin Dielectrics

JESD35-A

(Revision of JESD35)

APRIL 2001

JEDEC Solid State technology Association

Electronic Industries Alliance

NOTICE

JEDEC standards and publications contain material that has been prepared, reviewed, and approved through the JEDEC Board of Directors level and subsequently reviewed and approved by the EIA General Counsel.

JEDEC standards and publications are designed to serve the public interest through eliminating misunderstandings between manufacturers and purchasers, facilitating interchangeability and improvement of products, and assisting the purchaser in selecting and obtaining with minimum delay the proper product for use by those other than JEDEC members, whether the standard is to be used either domestically or internationally.

JEDEC standards and publications are adopted without regard to whether or not their adoption may involve patents or articles, materials, or processes. By such action JEDEC does not assume any liability to any patent owner, nor does it assume any obligation whatever to parties adopting the JEDEC standards or publications.

The information included in JEDEC standards and publications represents a sound approach to product specification and application, principally from the solid state device manufacturer viewpoint. Within the JEDEC organization there are procedures whereby an JEDEC standard or publication may be further processed and ultimately become an ANSI/EIA standard.

No claims to be in conformance with this standard may be made unless all requirements stated in the standard are met.

Inquiries, comments, and suggestions relative to the content of this JEDEC standard or publication should be addressed to JEDEC Solid State Technology Association, 2500 Wilson Boulevard, Arlington, VA 22201-3834, (703)907-7560/7559 or www.jedec.org

Published by
JEDEC Solid State Technology Association 2000
2500 Wilson Boulevard
Arlington, VA 22201-3834

PRICE: Please refer to the current
Catalog of JEDEC Engineering Standards and Publications or call Global Engineering Documents, USA and Canada (1-800-854-7179), International (303-397-7956)

PLEASE!

DON'T VIOLATE
THE
LAW!

JEDEC Solid State Technology Association
2500 Wilson Boulevard
Arlington, Virginia 22201-3834
or call (703) 907-7559

PROCEDURE FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS

CONTENTS

PROCEDURE FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS

Foreword

This document is intended for use in the MOS Integrated Circuit manufacturing industry fabrication processing and test and describes procedures developed for estimating the overall integrity of thin oxides. Three basic test procedures are described, the Voltage-Ramp (V-Ramp), the Current-Ramp (J-Ramp) and the Constant Current (Bounded J-Ramp) test. Each test is designed for simplicity, speed and ease of use.

The purpose of this document is to describe oxide test techniques for quick evaluation and control of oxide fabrication techniques. It does not specify acceptance or rejection criteria for any of the described procedures and therefore not intended to be used to predict MOS Integrated Circuit failure rates.

The material contained within this publication is formulated under the cognizance of JEDEC JC-14.2 Committee and approved by the JEDEC Board of Directors.

PROCEDURE FOR THE WAFER-LEVEL TESTING OF THIN DIELECTRICS

(From JEDEC Board Ballot JCB-99-24, formulated under the cognizance of JEDEC JC-14.2 Subcommittee on Wafer Level Reliability)

1 Scope

This document defines test procedures for the V-Ramp, J-Ramp and the Bounded J-Ramp oxide integrity tests. Included within this document are recommended data analysis methods and guidelines for statistical sampling.

2 Introduction

2.1 Overview

The thin dielectric integrity of MOS devices and circuits is an important reliability concern. Historically, thin oxide reliability has been driven by oxide defects. In general the intrinsic oxide lifetime is much longer than the use requirements, but defects can significantly reduce oxide lifetime. The procedures described herein were developed to estimate the integrity of a thin oxide and as a tool for driving constant improvement in the thin oxide process.

The test procedures described within this document should not used to predict failure rates of a semiconductor product but rather tools for process control of oxide integrity. In actual practice the oxide reliability of a semiconductor product is a complicated function of individual transistor duty cycles, transient voltage variation, the gate graded potential and series resistance in the gate load. These parameters are not considered within this document.

2.2 Choosing the appropriate stress procedures

Three test procedures are described within this document; a ramped voltage (V-Ramp), a ramped current (J-Ramp) and a constant current (Bounded J-Ramp) test. Each of these procedures is designed for simplicity, speed and ease of use and can be implemented at each point in the process from oxide formation onward.

The voltage ramp test (V-Ramp) starts at the use condition voltage or lower and ramps linearly from this value until oxide breakdown. The current density ramp test (J-Ramp) begins at a low value of current and ramps exponentially until oxide breakdown. The constant current test (Bounded J-Ramp) only rises to a specified current density level and it is maintained there until oxide breakdown.

2 Introduction (cont'd)

2.2 Choosing the appropriate stress procedures (cont'd)

V-Ramp tests are often applied to oxides where characterization of the defects at lower electric fields is important. On the other hand, since the J-Ramp begins at a voltage sufficient to produce measurable amounts of tunneling current (typically much higher than the starting voltage for a V-Ramp test), it can provide only very coarse segregation of the low field breakdowns, but can provide fine segregation of the high field breakdowns in much less time than a V-Ramp test. J-Ramp tests are often applied to small area test structures as a means of controlling an established process.

The Bounded J-Ramp (constant current) provides a very repeatable charge-to-breakdown (Q_{bd}) measurement where the current/current density is ramped to a specified level and then held until breakdown. The majority of the charge-to-breakdown in both the J-ramp and V-ramp tests occurs during the last few steps of testing. Thus timing, measurement conditions, step size can greatly influence the value of Q_{bd} using these tests. With the bounded J-Ramp, once a constant current value is reached, each increment contributes approximately the same charge to the total value of Q_{bd} reducing the dependence on testing equipment. For these reasons, comparisons of Q_{bd} should be performed using the Bounded J-Ramp.

As a result of this difference in the speed and field resolution of the above tests, there are applications where each one might be more appropriate. The J-Ramp test typically takes less time to determine defect density than a V-Ramp test. So the J-Ramp might be favored if large sample size and throughput are important. The Bounded J-Ramp has better Q_{bd} resolution. When low field extrinsic information is desired, then the V-Ramp may be a better choice. However, all of these tests will allow resolution between defective (extrinsic) and non-defective (intrinsic) oxide test structures.

3 Terms and definitions

The following symbols are used in this document. They have been listed alphabetically for the convenience of the reader.

a_{oxide} (cm^2): Thin oxide gate area.

compliance: The test equipment maximum current or voltage forcing capability. Often the user can specify a compliance limit for a particular test. In this case the test instrumentation will not exceed this compliance limit during the test procedure.

3 Terms and definitions (cont'd)

***E* (V/cm):** E is the estimated oxide electric field. The general formula for E is:

$$E = V / T_{ox},$$

where V is the voltage and T_{ox} is the estimated oxide thickness, as determined by a consistent, documented method. The method (or a reference to the documented standard) must be included in the data report.

***E_{bd}* (V/cm):** The estimated oxide electric field just prior to the detection of breakdown (see Annex C).

J (A/cm^2): The oxide current density calculated by dividing the oxide current by the oxide area (Aoxide).

Qbd (Coulombs): The accumulated charge passing through the oxide prior to breakdown is defined as:

$$Q_{bd} = \int_{t=0}^{t=t_{bd}} I(t)dt \qquad (2)$$

where t is time. The Q_{bd} is calculated as the integral from t = 0 to t = t_{bd} where t_{bd} is the last measurement time at the step just prior to breakdown.

qbd (C/cm^2): The accumulated charge density, passing through the oxide at the detection of breakdown. Calculated as:

$$q_{qb} = \frac{Q_{bd}}{A_{oxide}} \qquad (3)$$

4 V-ramp test procedure

4.1 Test configuration

The voltage-ramp (V-RAMP) test is performed on an oxide capacitor by applying a voltage between the gate electrode (typically polysilicon or aluminum) and bulk electrode (typically substrate or well) with all other diffusions and wells connected to substrate. It is recommended that the gate voltage polarity should bias the device into accumulation to minimize inversion capacitance effects but inversion can be used if the test structure design or conditions such as heat or light illumination provides a source of minority carriers to the inverted layer. Although these procedures are applicable to measurements at other operating temperatures these procedures are typically performed at room temperature (25 ± 5 ºC).

The oxide capacitor test structure should be designed so that parasitic series resistance effects are minimized. High series resistance can severely impact the accuracy of these measurements. This is especially true for high current oxide breakdowns where large series resistance voltage drops occur. A second requirement of the capacitor test structure is that probe pads should not exist over the oxide under stress. Mechanical stress caused by probing pads over oxides can result in device damage and inaccurate defect density measurements.

The following sections describe the details of the V-Ramp measurement. This measurement is performed in three parts. First, a pre-oxide current test checks for an 'initial' failure. After this test, a voltage ramp is performed until oxide breakdown. Finally a post oxide current test determines the final state of the oxide structure.

4.2 V-Ramp input and output parameters

The V-Ramp input and output parameters are listed in Table 4.1 and Table 4.2, respectively. Table 4.1 defines the input parameters required to set up the V-Ramp test and also defines input parameter guidelines. Table 4.2 defines the V-Ramp output parameters. Optional output parameters include V_{crit} and V_{box} (see Table 4.2 for definitions).

4.2 V-Ramp input and output parameters (cont'd)

Table 4.1 — Input parameters for the V-Ramp test procedure

Input	Units	Comments
V_{use}	V	Oxide voltage under normal operating conditions, typically the power supply voltage of the process. This voltage is used to measure pre- and post voltage ramp oxide current.
I_{init}	A	Oxide breakdown failure current when biased at V_{use}. Typical value is $10\mu A/cm^2$ and may change depending on oxide area. For maximum sensitivity the specified value should be well above the worse case oxide current of a "good" oxide and well above the "noise level" of the measurement system. Higher values must be specified for ultra-thin oxides because of direct tunneling effects.
V_{start}	V	Starting voltage for voltage ramp. Typical value is V_{use}.
V_{step}	V	Voltage ramp step height. This value has a maximum value of 0.1 MV/cm. For example, the maximum value can be calculated using T_{ox}*0.1 MV/cm, where T_{ox} is in units of centimeters. This is 0.1 V for a 10 nm oxide.
t_{step}	s	Voltage ramp step time. The Voltage ramp step time is determined from the Ramp-rate and V_{step}. The step time should be less than or equal to 0.1sec.
Ramp-rate	V/s	The Ramp-rate is specified at 1.0 MV/cm per second. For example, the ramp-rate should be set to T_{ox}*1.0 MV/cm-sec where T_{ox} is in centimeters. This is 1 V/s for a 10.0 nm oxide.
I_{crit}	A	At least 10 times the test system current measurement noise floor. This oxide current is the minimum value used in determining the change of slope breakdown criteria
I_{box}	A	An optional measured current level for which a stress voltage is recorded. This value provides an additional point on the current-voltage curve. A typical value is 1 μA.
I_{bd}	A	Oxide current breakdown criteria. I_{bd} is obtained from I-V curves and is the oxide current at the step just prior to breakdown.
q_{max}	C/cm^2	Maximum accumulated oxide charge per oxide area. Used to terminate a test where breakdown occurred but was not detected during the test.
V_{max}	V	The maximum voltage limit for the voltage ramp. This limit is specified at 30 MV/cm for oxides less than 20 nm thick and 15 MV/cm for thicker oxides. For example, V_{max} can be estimated from T_{ox}*30 MV/cm where T_{ox} is in centimeters. This is 35 V for a 10.0 nm oxide.

4.2 V-Ramp input and output parameters (cont'd)

Table 4.2 — Output parameters for the V-Ramp test procedure

Outputs	Units	Comments
$I_{use\text{-}pre}$	A	Measured voltage ramp oxide current at V_{use} prior to starting the ramp.
Q_{bd}	C	Charge-to-breakdown. Cumulative charge passing through the oxide prior to breakdown.
V_{crit}	V	Applied voltage at the step where the oxide current exceeds I_{crit}.
V_{box}	V	Applied voltage at the step where the oxide current exceeds I_{box}.
V_{bd}	V	Applied voltage at the step just before oxide breakdown
q_{bd}	C/cm^2	Charge-to-breakdown density.
$I_{use\text{-}post}$	A	Oxide current at V_{use} after the ramp.
Failure Type	-	Failure type as determined in Table 4.3.

4.3 Pre-Ramp oxide current test

Figure 4.1 displays a basic V-Ramp flow diagram. The V-Ramp test procedure begins by performing an oxide current measurement to validate the low field performance of the test device. This test applies a gate bias V_{use} and measures the oxide current $I_{use\text{-}pre}$. If $I_{use\text{-}pre}$ exceeds the fail current (I_{init}) the oxide is considered an 'initial' failure (see 4.5 for failure categories) and testing terminates. Figure 4.2 shows a more detailed V-Ramp flow diagram to aid coding the procedure in software.

4.4 Ramp voltage stress

After the pre-test a linear or stepped voltage ramp is applied to the oxide test device. The voltage starts at V_{start} and ramps at a predefined ramp rate, or is stepped by the voltage V_{step} for duration t_{step}. During the voltage ramp the current is monitored at least as often as t_{step}. For the stepped voltage ramp the current measurement should be delayed at each voltage step to allow displacement currents to settle. This implies that t_{step} must be longer than the instrument's settling time plus the measurement time of the test system. At each voltage step the measured oxide current should be compared to the oxide breakdown criterion. If oxide breakdown has not occurred, the accumulated oxide charge should be recalculated using Equation 4 below:

$$Q_{bd} = \sum_{i=1}^{i=n} I_{meas}(i) * t_{step} \qquad (4)$$

where $I_{meas}(i)$ is the measured oxide current at each voltage step n, t_{step} is the step duration and n the total number of voltage steps just prior to breakdown. If oxide breakdown has been detected, the voltage ramp should be stopped and the final post-ramp device test performed (see 4.5). Figure 4.3 illustrates a typical voltage ramp test.

4.4 Ramp voltage stress (cont'd)

Other test conditions besides oxide breakdown may stop the voltage ramp test. These include reaching the maximum specified test voltage V_{max}, current compliance of test system, or exceeding the maximum specified oxide charge density q_{max}. If either of these conditions occur, a measurement or test condition problem may exist (e.g. improper contact to the gate/bulk, high series resistance, or invalid specified V_{max} or q_{max} values).

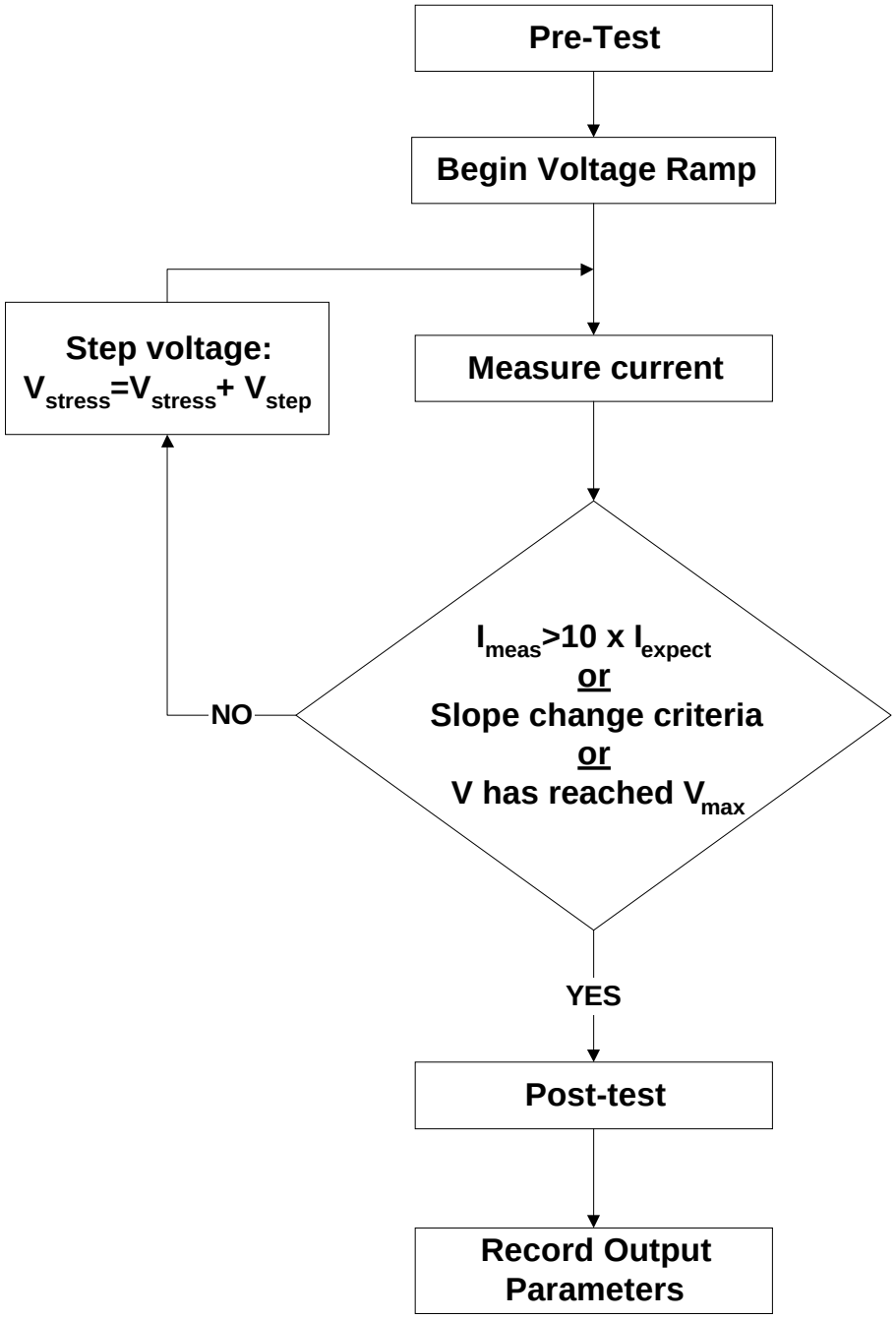
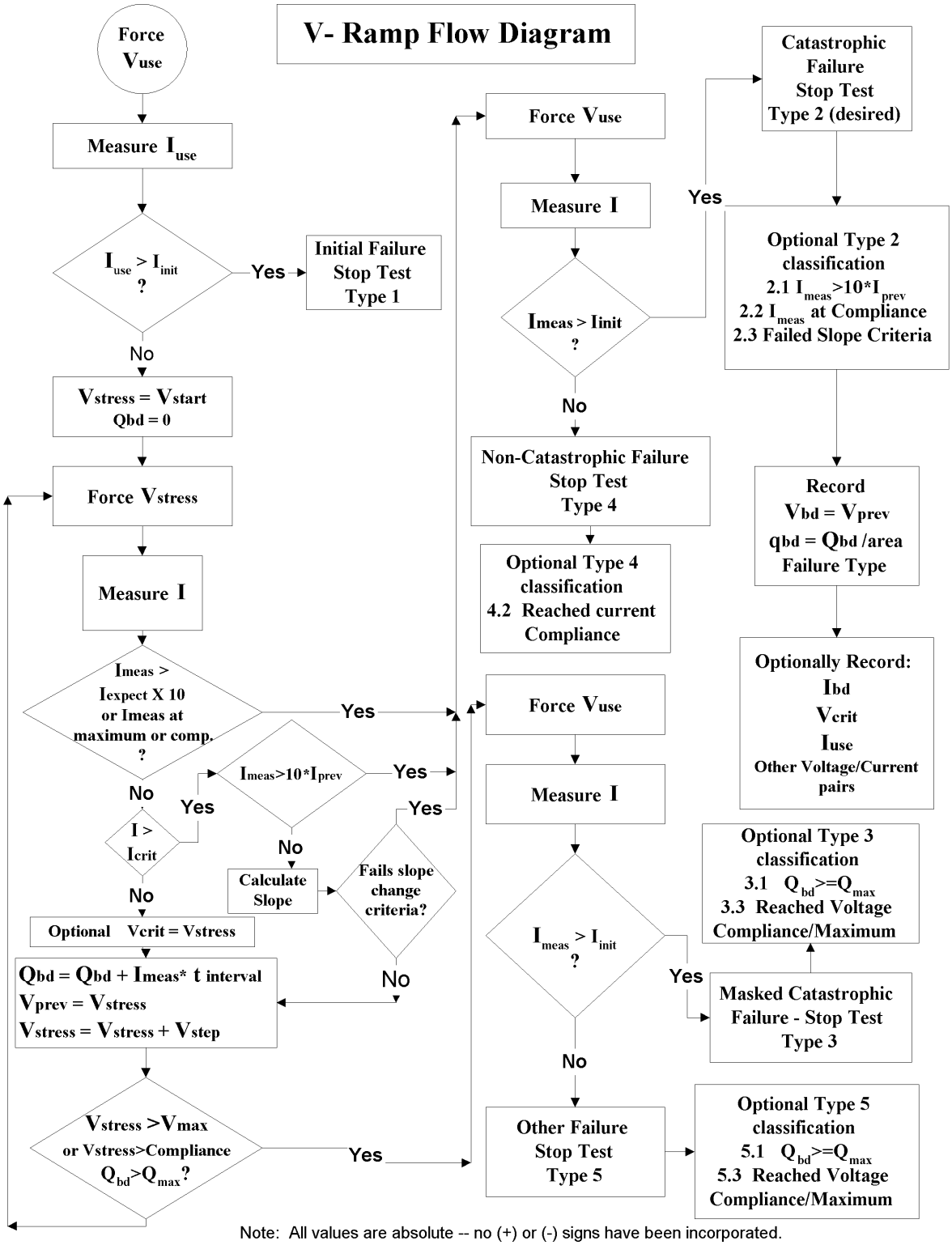


Figure 4.1 — Basic voltage-ramp flow diagram

4.4 Ramp voltage stress (cont'd)



Note: All values are absolute -- no (+) or (-) signs have been incorporated.

Figure 4.2 — Detailed voltage-ramp flow diagram

4.4 Ramp voltage stress (cont'd)

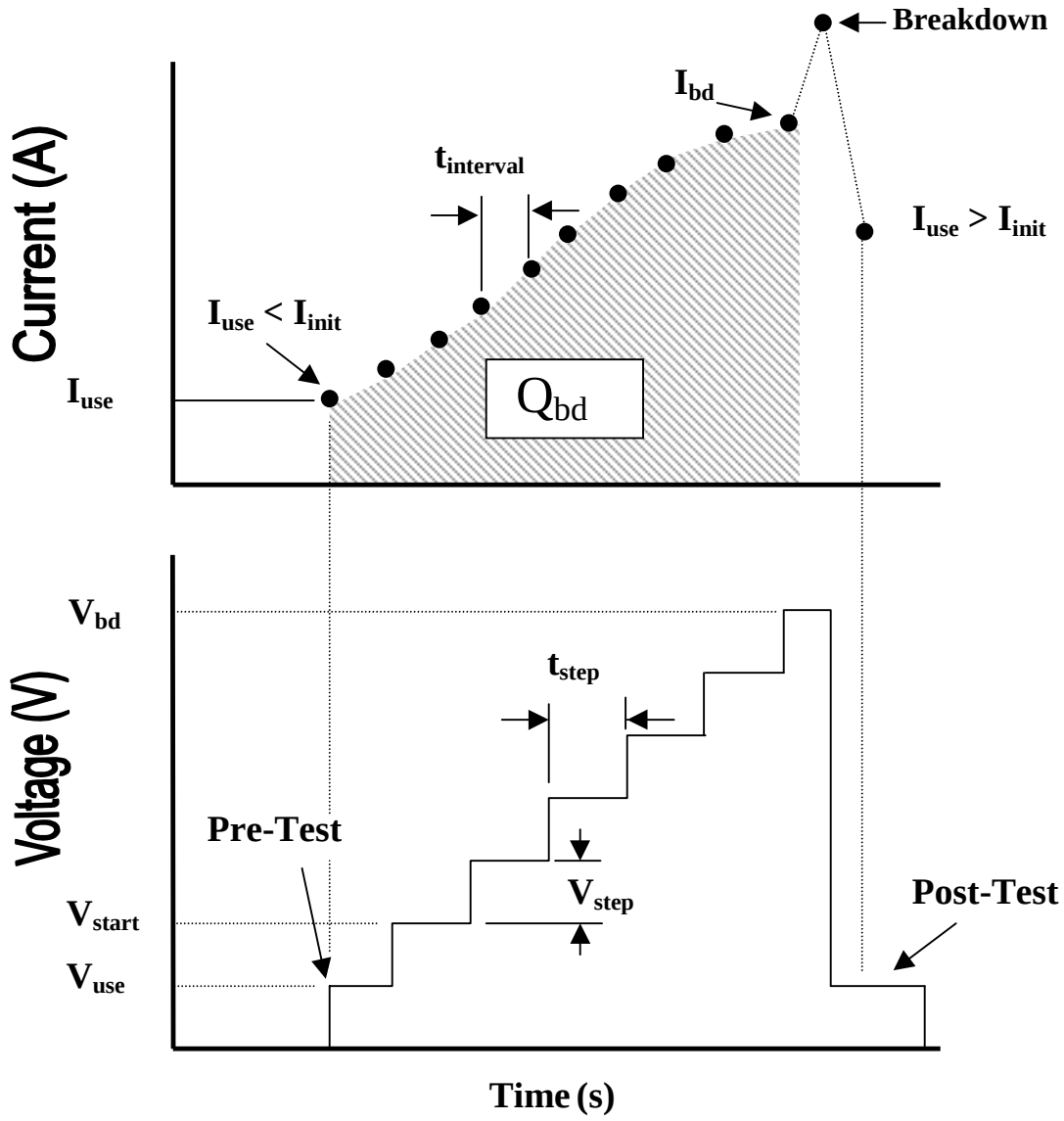


Figure 4.3 — Diagram of typical voltage-ramp test

4.4.1 Oxide breakdown criteria

Oxide breakdown criteria may be specified in several ways. One of the simplest is a measured current that exceeds a specified failure current. Unfortunately, device series resistance can limit oxide current to values below the specified level. It is therefore essential that the oxide failure criteria be carefully specified. Described below are the oxide failure criteria. Oxide failure is defined when one of the following criterion is satisfied.

4.4.1 Oxide breakdown criteria (cont'd)

4.4.1.1 Absolute current level

This criteria specifies that breakdown occurs when the magnitude of the oxide current exceeds the breakdown current level I_{bd} (limited by the current compliance of the test system). I_{bd} is defined as 10 times the expected oxide current based on device I-V curves. Typical values range from 20 to 30 A/cm^2. This value must be carefully selected. If I_{bd} is too small the current ramp will stop before the true breakdown event while if I_{bd} is too large the breakdown may never be detected because device series resistance limits the breakdown current to values less than I_{bd}.

4.4.1.2 Change in slope of oxide current versus voltage

This criteria specifies that oxide breakdown occurs when the logarithmic slope of I_{meas} vs V_{stress} curve increases by a factor greater than the previously calculated slope. Typical exit values are an increase in slope that is greater than 2.5 to 5 times the previous slope value with 3 being the recommended value. Measurement noise restricts use of this failure criterion to oxide currents at least 10 times the noise floor of the instrument.

The previous logarithmic slope ($Slope_{prev}$) is calculated from

$$Slope_{prev} = \frac{abs(\ln(abs(I(n-1))) - \ln(abs(I(n-2))))}{V(n-1) - V(n-2)} \quad (5)$$

where I(n-1), V(n-1) and I(n-2), V(n-2) are the measured currents and voltages of the previous two data points and "*abs*" is the absolute value. The most recent slope ($Slope_{new}$) is calculated using Equation 6.

$$Slope_{new} = \frac{abs(\ln(abs(I(n))) - \ln(abs(I(n-1))))}{V(n) - V(n-1)} \quad (6)$$

where I(n), V(n) and I(n-1), V(n-1) are the measured currents and voltages of the most recent and previous data points, respectively. For example, an oxide failure is detected if the most recent measured slope ($slope_{new}$) is 3 times greater the previous calculated slope ($slope_{prev}$).

4.5 Post-ramp oxide current test

Once the voltage ramp is completed, following the detection of breakdown defined in 4.4.1 or if the test is terminated for the conditions discussed in 4.4, a post ramp current test at V_{use} is used to determine the final state of the test device. Based on these and the previous test results the oxide failure category is determined. See Table 4.3 for the list of oxide failure categories.

4.6 Data recording

For all catastrophic failures (desired failure category, see Table 4.3) record the following information as outlined below.

- V_{bd} - the oxide breakdown voltage (V_{bd}).
- q_{bd} - the accumulated oxide breakdown charge density.
- Failure category – the oxide failure mode as defined in 4.7.

In addition it is recommended that the following parameters be recorded:

- I_{bd} - the oxide breakdown current.
- V_{crit} – the measured gate voltage (V_{crit}) at an oxide current (I_{crit}).
- V_{box} – the gate voltage that yields an oxide current at I_{box}.

$I_{use\text{-}pre}$ and $I_{use\text{-}post}$ – the pre- and post-test oxide current at V_{use} can be recorded for debugging test coding and equipment.

4.7 Oxide failure categories

Because of the complexity of the oxide test procedure, five possible oxide failure types can occur. These failure types are listed in Table 4.3 and discussed in this section:

Type 1 Failure - Initial Failure Class A
Initial oxide current exceeds failure criteria. Device is “shorted”.

Type 2 Failure - Catastrophic Failure
Breakdown is detected both during the voltage ramp and during the post-ramp oxide leakage test. This is the desired outcome. Other failure types indicate faults in the test.

Type 3 Failure - Masked Catastrophic Failure
Oxide breakdown is not detected during the voltage ramp but the detected in the post-ramp oxide leakage test.

Type 4 Failure - Non-Catastrophic Failure
Oxide breakdown is detected during the voltage ramp but not in the post-ramp oxide leakage test.

Type 5 Failure - Other Failures
Oxide breakdown is not detected during the voltage ramp or in the post-ramp oxide leakage test.

4.7 Oxide failure categories (cont'd)

Table 4.3 — Oxide failure categories

Stress failure type	Initial test	Ramp test	Post test
Initial (Type 1)	Fail	N/A	N/A
Catastrophic (Type 2)	Pass	Fail	Fail
Masked Catastrophic (Type 3)	Pass	Pass	Fail
Non-catastrophic (Type 4)	Pass	Fail	Pass
Others (Type 5)	Pass	Pass	Pass

NOTE Pass in the Initial-test indicates that the initial oxide current did not exceed the failure criteria, i.e., the oxide was not "shorted". Pass in the Post-test also indicates that the oxide current did not exceed the failure criteria, i.e., it was not "shorted". Pass in the Ramp test indicates that oxide breakdown was not detected with one of the failure criteria specified in 4.4.1.

5 J-Ramp test procedure

5.1 Test configuration

The J-Ramp oxide test should be performed with the device biased in accumulation, the diffusions connected to the substrate and the test temperature at 25 $\pm$ 5 ºC. As was discussed (see 4.1) these constraints can be relaxed under certain conditions.

5.2 J-Ramp input and output parameters

The J-Ramp input and output parameters are listed in Table 5.1 and Table 5.2, respectively. Table 5.1 defines the input parameters required to set up the J-Ramp test and also defines input parameter guidelines. Table 5.2 defines the J-Ramp output parameters.

5 J-Ramp test procedure (cont'd)

5.2 J-Ramp input and output parameters (cont'd)

Table 5.1 — Input parameters for the J-Ramp test procedure

Input	Units	Comments
V_{use}	V	Oxide voltage under normal operating conditions, typically the power supply voltage or normal use voltage of the process. This voltage is used to measure pre- and post oxide current.
I_{init}	A	Oxide breakdown failure current when biased at V_{use}. Typical value is 10 $\mu A/cm^2$ and may change depending on oxide area. For maximum sensitivity the specified value should be well above the worse case oxide current of a "good" oxide and well above the "noise level" of the measurement system. Higher values must be specified for ultra-thin oxides because of direct tunneling effects.
I_{start}	A	Starting current for current ramp. Typical value is I_{init}.
F		Current multiplier between two successive current steps.
t_{step}	s	Current ramp step time.
I_{max}	A	Maximum ramp current.
V_{max}	V	The maximum voltage limit for the voltage ramp. This limit is specified at 30 MV/cm for oxides less than 20 nm thick and 15 MV/cm for thicker oxides. For example, V_{max} can be estimated from T_{ox}*30 MV/cm where T_{ox} is in centimeters. This is 35 V for a 10.0 nm oxide.
q_{max}	C/cm^2	Maximum accumulated oxide charge per oxide area. Used to terminate a test where breakdown occurred but was not detected during the test.

Table 5.2 — Output parameters for the J-Ramp test procedure

Outputs	Units	Comments
$I_{use\text{-}pre}$	A	Measured voltage ramp oxide current at V_{use} prior to starting the ramp.
Q_{bd}	Coul.	Charge-to-breakdown. Cumulative charge passing through the oxide prior to breakdown.
V_{bd}	V	Applied voltage at the step just before oxide breakdown
q_{bd}	C/cm^2	Charge-to-breakdown density.
$I_{use\text{-}post}$	A	Oxide current at V_{use} after the ramp.
Failure Type	-	Failure types are listed in Section 5.8.

5 J-Ramp test procedure (cont'd)

5.3 Pre-Ramp oxide test

Figure 5.1 displays the basic J-Ramp test flow diagram. In the case of the J-Ramp test it is recommended that both a voltage and current test be used verify the functionality of the tested device. In this case there are two classes of Type 1 failures. In the voltage test the use voltage V_{use} is applied to the device and the oxide current measured (see 4.1). If the measured current exceeds I_{init} an "initial" device failure (Type 1, Class A failure "short") is indicated and testing terminates.

During a second pre-test I_{init} (typical value 1 μA) is applied to the test device and the voltage sustained across the device measured. If the measured voltage is less than V_{use} an "initial" device failure (Type 1, Class B failure) is indicated and testing terminates. It is important to note that the measurement delay time between current force and voltage measure must be long enough for the system to reach the correct equilibrium initial voltage. This may take several seconds for low forcing currents.

Once the capacitor passes the initial test, the J-Ramp test should start immediately. The initial stress current should be large enough to yield a short initial test time but small enough to detect early oxide failures. Initial stress current values often depend on test structure area, oxide thickness and equipment capabilities.

Figure 5.2 shows a more detailed J-Ramp flow diagram to aid coding the procedure in software.

5 J-Ramp test procedure (cont'd)

5.3 Pre-Ramp oxide test (cont'd)

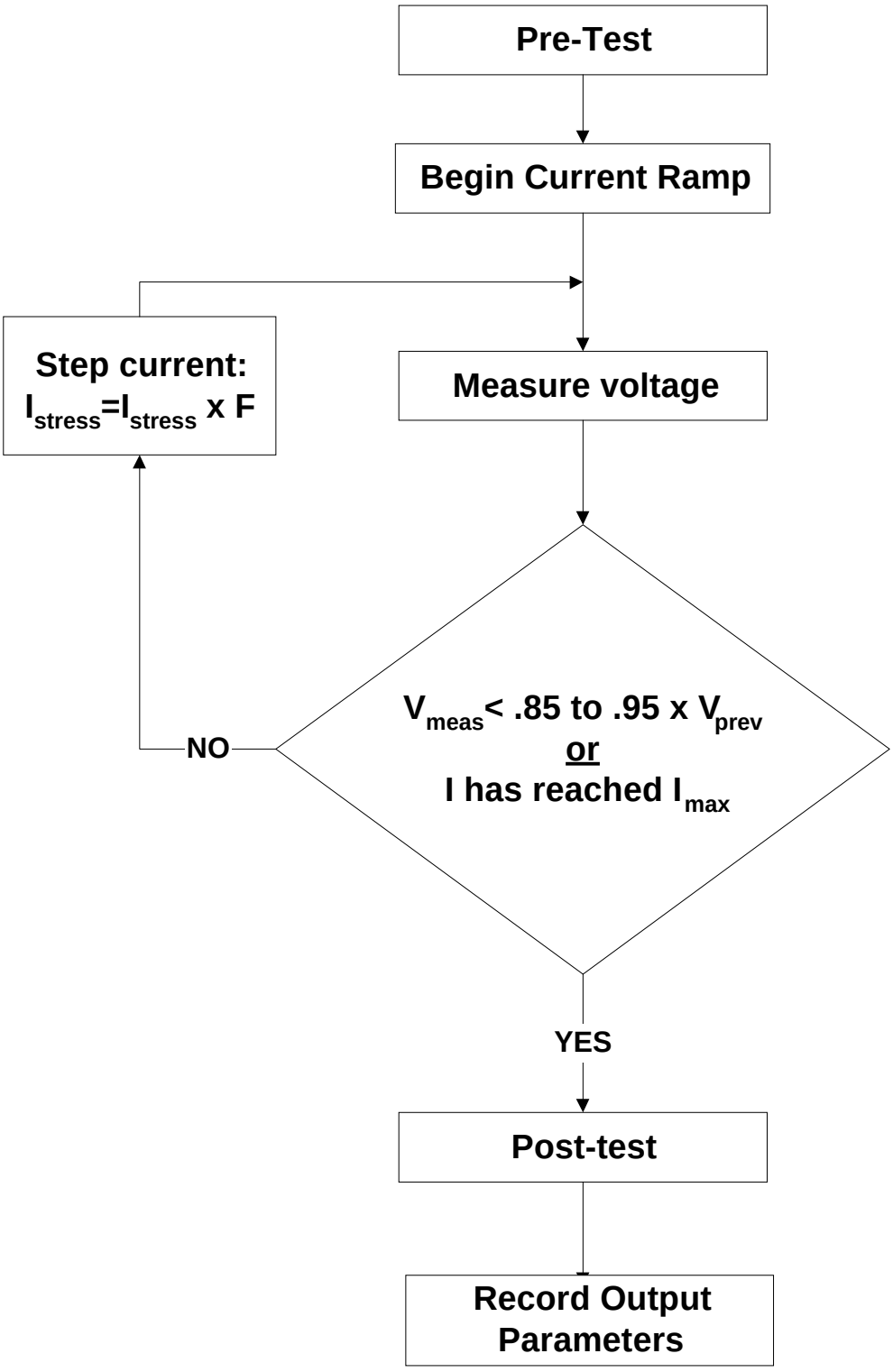
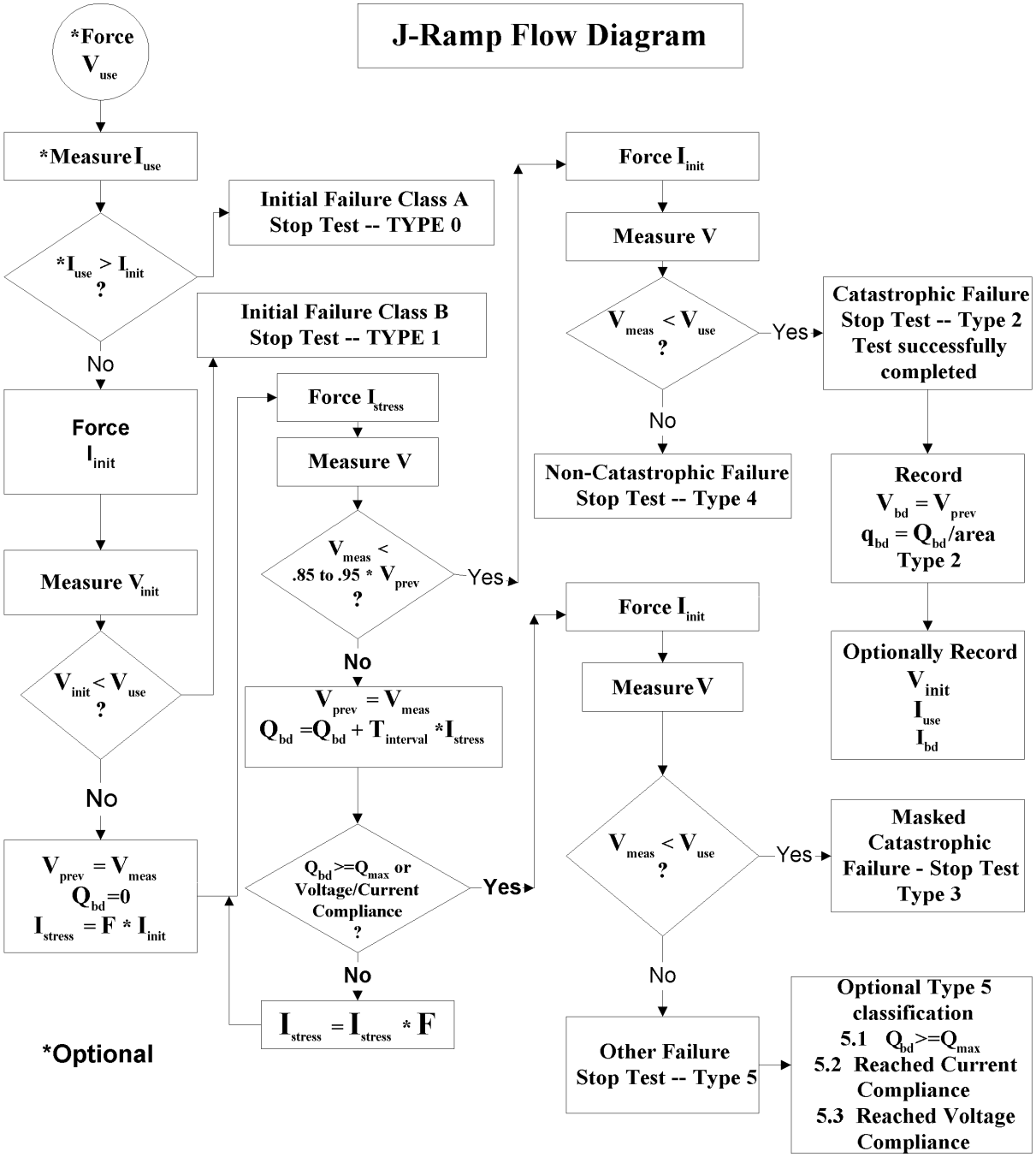


Figure 5.1 — Basic J-Ramp flow diagram

5 J-Ramp test procedure (cont'd)

5.3 Pre-Ramp oxide test (cont'd)



NOTE All values are absolute - no (+) or (-) signs have been incorporated

Figure 5.2 — Detailed J-Ramp flow diagram

5 J-Ramp test procedure (cont'd)

5.4 J-Ramp stress test

A stepped current consistent with biasng the device in accumulation should be applied while the voltage across the oxide continuously (or at short, evenly spaced intervals) monitored. The current should be stepped in logarithmic intervals such that the ratio of two successive steps is a constant factor, F (F-factor). The J-Ramp should be terminated if the most recent measured oxide voltage decreases below a certain fraction (typically 0.85-0.95) of the highest previously measured oxide voltage. Other test conditions may terminate the J-Ramp test besides oxide breakdown. These test conditions include reaching the maximum specified test voltage V_{max} or stress current I_{max} or exceeding the maximum accumulated oxide charge density q_{max}. If either of these conditions occur a measurement or test condition problem may exist.

5.4.1 F-factor

F-factor is defined as the constant multiplier between two successive current steps. The F-factor value affects the precision of Q_{bd} measurements. The larger the F-factor the courser the Q_{bd} determination. The following table shows the effect F-factor on accumulated Q_{bd} for the last current step

S	F	$Q_{laststep}$
2	3.162	68.38%
5	1.585	36.90%
10	1.259	20.57%
25	1.096	4.50%
50	1.047	3.80%

where S is the number of current steps per decade, F is the F-factor and $Q_{laststep}$ is the percentage of the total Q_{bd} that is accumulated in the last current step of the J-Ramp test.

5.4.2 J-Ramp test characteristics

The following table defines the J-Ramp test characteristics:

Current ramp rate	1 current decade/500 ms
Maximum time between voltage measurements	Lesser of 50 ms and once per current step
Maximum charge density	50 C/cm^2
Maximum field	25 MV/cm (Tox < 20 nm) 15 MV/cm (Tox >= 20 nm)
Maximum F-factor (F)	Square root of 10 (approx. 3.2)
Step duration	Must be uniform and conform to ramp rate
Exit Criteria	Typically 0.85-0.95 of highest previously measured voltage

5.4 J-Ramp stress test (cont'd)

5.4.2 J-Ramp test characteristics (cont'd)

J-Ramp should only be performed on oxides that survive the initial test. The starting current can be F times $I_{use\text{-}pre}$ (the current used in the pre-ramp oxide test) or lower current. Figure 5.3 shows a schematic of a typical J-Ramp stress-measurement curve. The structure is considered broken down if the most recent measured voltage is less than a certain factor (typical values are 0.85 - 0.95) times the highest previously measured voltage. For ultra-thin oxides < 5 nm the recommended exit criteria may require adjustment.

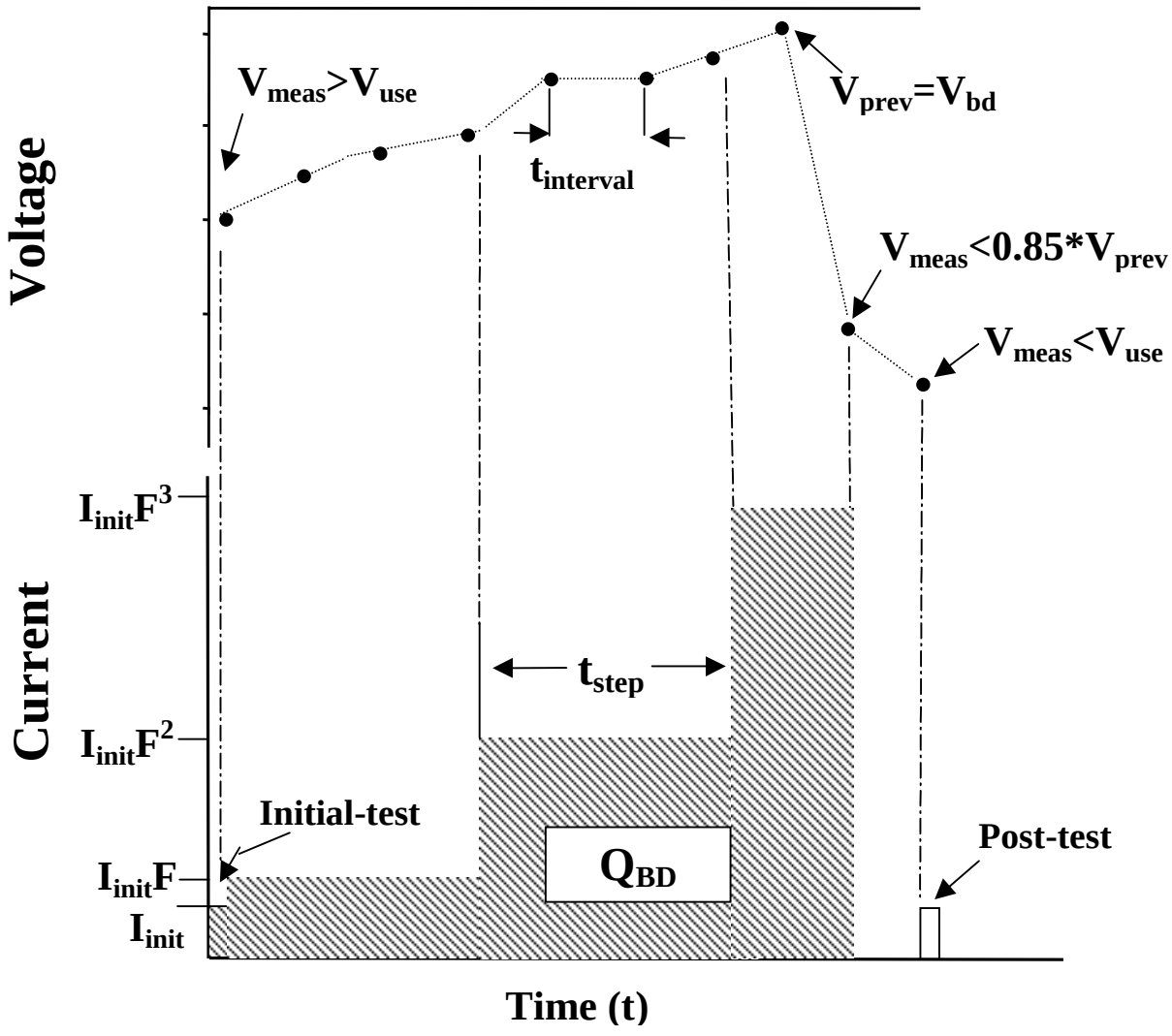


Figure 5.3 — Diagram of typical J-Ramp test

5 J-Ramp test procedure (cont'd)

5.5 Bounded J-Ramp

A variation of the J-Ramp test is the bounded J-Ramp test. In the bounded J-Ramp test the current is ramped to a constant value (prevents voltage overshoot) and is held at this value for the duration of the test. The current ramp should be performed in the same manner as the J-Ramp test (see 5.3). Before applying each current step the magnitude of the stress current should be compared to the specified holding current. If the holding current is exceeded the bounded current (I_{bound}) should be applied. A current density of 0.1 to 0.5 A per square centimeter will typically yield consistent results and a reasonable test duration. Empirical measurements have shown that lower current levels yield higher Q_{bd} and tighter measurement distributions.

The failure criteria and categories for the bounded current test are identical to the J-Ramp test (see 5.3 and 5.6). Figure 5.4 shows a detailed flow diagram of the bounded J-Ramp test.

5 J-Ramp test procedure (cont'd)

5.5 Bounded J-Ramp (cont'd)

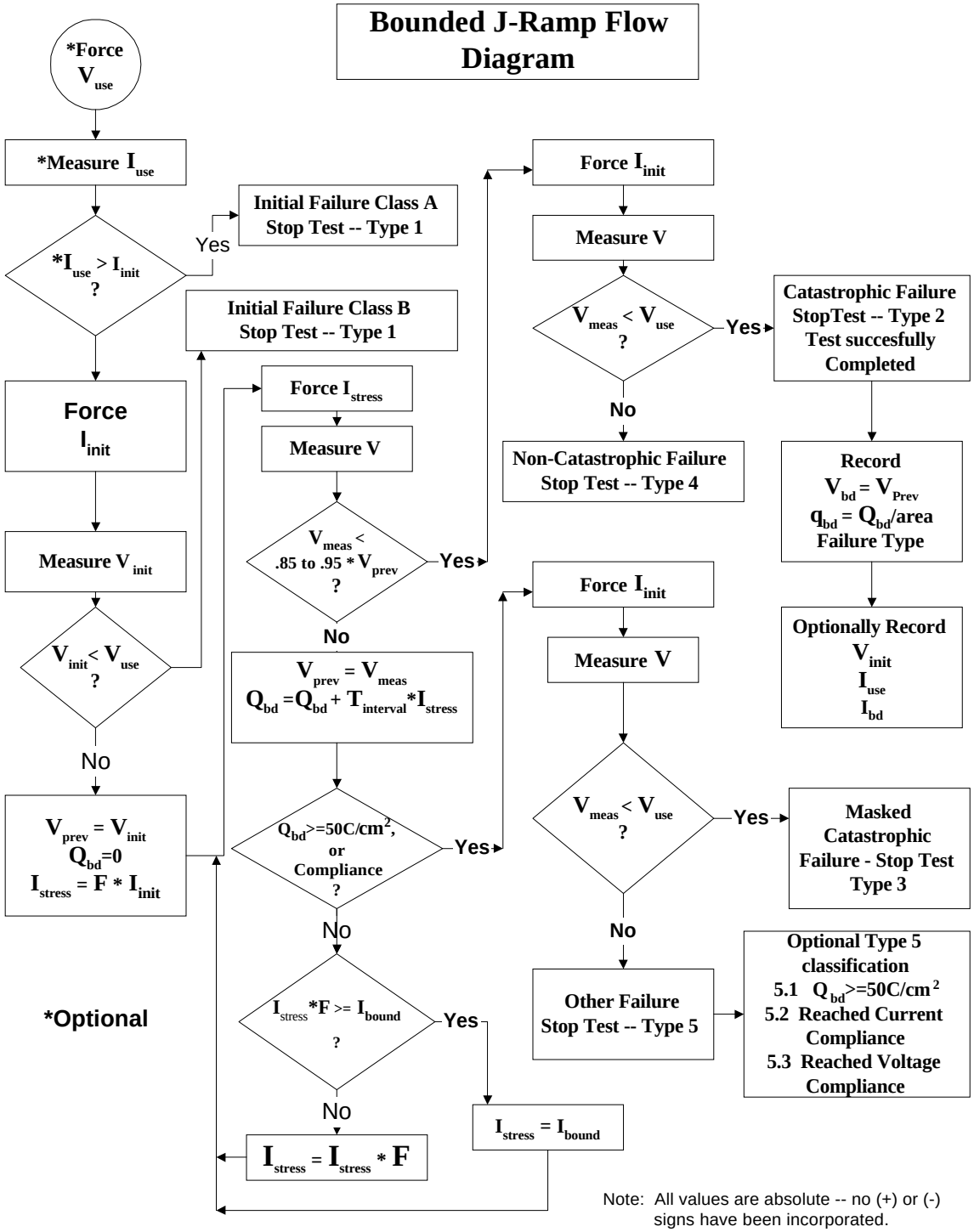


Figure 5.4 — Detailed bounded J-Ramp flow diagram

5 J-Ramp test procedure (cont'd)

5.6 Post-ramp oxide test

Once the current ramp is complete the test device is re-tested in the same manner as described in 5.3 to determine the final state of the test device. Based on this post-test and the previous test results an oxide failure category is specified. See 5.8 for the oxide failure categories.

5.7 Data recording

For all catastrophic failures record at least:

- V_{bd} - the oxide breakdown voltage (V_{bd}). The breakdown voltage is the maximum voltage attained during testing before breakdown.

- q_{bd} – Charge-to-breakdown density.

- Failure category – the oxide failure type as defined in Section 4.8.

In addition it is recommended that the following parameters be recorded:

- I_{bd} - the oxide breakdown current.

- V_{crit} – the measured gate voltage (V_{crit}) at an oxide current (Icrit).

- V_{box} – the gate voltage that yields an oxide current at I_{box}.

$I_{use\text{-}pre}$ and $I_{use\text{-}post}$ – the pre- and post-test oxide current at Vuse can be recorded for debugging test coding and equipment.

5 J-Ramp test procedure (cont'd)

5.8 Oxide failure categories

Because of the complexity of the oxide test procedure, five possible oxide failure types can occur. These failure types are listed in Table 5.3 and discussed in this section:

Initial Failure Class A
Initial oxide current exceeds failure criteria. Device is "shorted".

Initial Failure Class B
Initial oxide voltage is less then V_{use} with I_{init} applied.

Type 2 Failure - Catastrophic Failure
Breakdown is detected both during the voltage ramp and during the post-ramp oxide leakage test. This is the desired outcome. Other failure types indicate faults in the test.

Type 3 Failure - Masked Catastrophic Failure
Oxide breakdown is not detected during the voltage ramp but the detected in the post-ramp oxide leakage test.

Type 4 Failure - Non-Catastrophic Failure
Oxide breakdown is detected during the voltage ramp but not in the post-ramp oxide leakage test.

Type 5 Failure - Other Failures
Oxide breakdown is not detected during the voltage ramp or in the post-ramp oxide leakage test.

Table 5.3 — Oxide failure categories

Stress Failure Category	Initial Test	Ramp Test	Post Test
Initial (Type 1)	Fail	N/A	N/A
Catastrophic (Type 2)	Pass	Fail	Fail
Masked Catastrophic (Type 3)	Pass	Pass	Fail
Non-catastrophic (Type 4)	Pass	Fail	Pass
Others (Type 5)	Pass	Pass	Pass

NOTE Pass in the Initial-Test indicates that the initial oxide current did not exceed the failure criteria, i.e., the oxide was not "shorted". Pass in the Post-Test also indicates that the oxide current did not exceed the failure criteria, i.e., it was not "shorted". Pass in the Ramp Test indicates that oxide breakdown was not detected with one of the failure criteria specified in 4.4.1.

6 References

1. D. S. Peck and O. D. Trapp, *Accelerated Testing Handbook*, Technology Associates, 1981.

2. K. Ishikawa, *Guide to Quality Control*, Asian Productivity Organization, 1982.

3. EIA/JEDEC Standard 19, *General Standard for Statistical Process Control (SPC)*, Electronic Industries Association, Washington D.C. 1989.

4. R. Degraeve, J.L. Ogier, R. Bellens, Ph. Roussel, G. Groeseneken, H.E. Maes, *On the Field Dependence of Intrinsic and Extrinsic Time-Dependent Dielectric Breakdown, IRPS Proceedings*, p. 44, 1996.

5. ASTM F-17-71 *Test Method for Evaluating Gate Oxide Integrity by Voltage Ramp Technique*, American Society for Testing and Materials, West Conshohocken, PA, 1998.

6. EIA/JEDEC Standard 35-1, *General Guidelines for Designing Test Structures for the Wafer-Level Testing of Thin Dielectrics*, Electronics Industries Association, Washington, D.C., 1995.

7. EIA/JEDEC Standard 35-2, *Test Criteria for the Wafer-Level Testing of Thin Dielectrics*, Electronics Industries Association, Washington, D.C., 1995.

Annex A Supplemental data analysis

A.1 Overview

This annex is not a formal part of the test procedures but is included for purposes of information.

Analysis of the data obtained from thin dielectric wafer level testing is the same regardless of whether the data was obtained using a V-Ramp or a J-Ramp test. Consequently, the analysis procedures described herein do not distinguish between these two test methods. A.2 discusses analysis techniques for monitoring and controlling oxide reliability, while A.3 discusses techniques for analyzing the source of oxide defects.

In all of these analysis techniques, no target values are given. This has been done intentionally to acknowledge that the proper way to maintain reliability is to continuously drive the monitored values closer and closer to their ideal values. It is also recognized that different applications have different reliability requirements.

A.2 Data analysis

The use of the procedure about to be described is recommended when only catastrophic and initial failures are found during the tests, or when other types of failures are found and can be shown to resemble catastrophic failures. Refer to 4.5 and 5.5 for the definitions of the failure categories. The additional failure types referenced in the above sections are typically due to some artifact of the structure or the test that makes the data suspect. For example, in the V-Ramp test, masked catastrophic failures may be due to an insufficiently high current compliance of the power supply or to excessive series resistance of the structure. Similarly, non-catastrophic failures may result from oxide healing, and the "other" types of failures could be caused by poor probe-to-pad contacts or to open circuits elsewhere in the tester or structure. It should be remarked that ideally only catastrophic failures should be obtained. The presence of other failure categories suggests that either defect elimination work or test modification is needed.

Analysis of the breakdown voltage data is predicated on the concept that for each failure, the breakdown voltage, V_{bd}, can be translated to an estimated breakdown electric field, E_{bd}, by dividing the voltage by the oxide thickness. The data analysis begins by plotting the cumulative breakdown distribution versus E_{bd} on normal probability paper. Often, such a plot results in a bimodal or other multi-modal distribution. Figure A.1 shows a typical bimodal distribution, displaying an extrinsic and an intrinsic population. Analysis techniques are available that allow the separation of this distribution into two single mode distributions, namely the intrinsic and the extrinsic distributions [1].

Annex A Supplemental data analysis (cont'd)

A.2 Data analysis (cont'd)

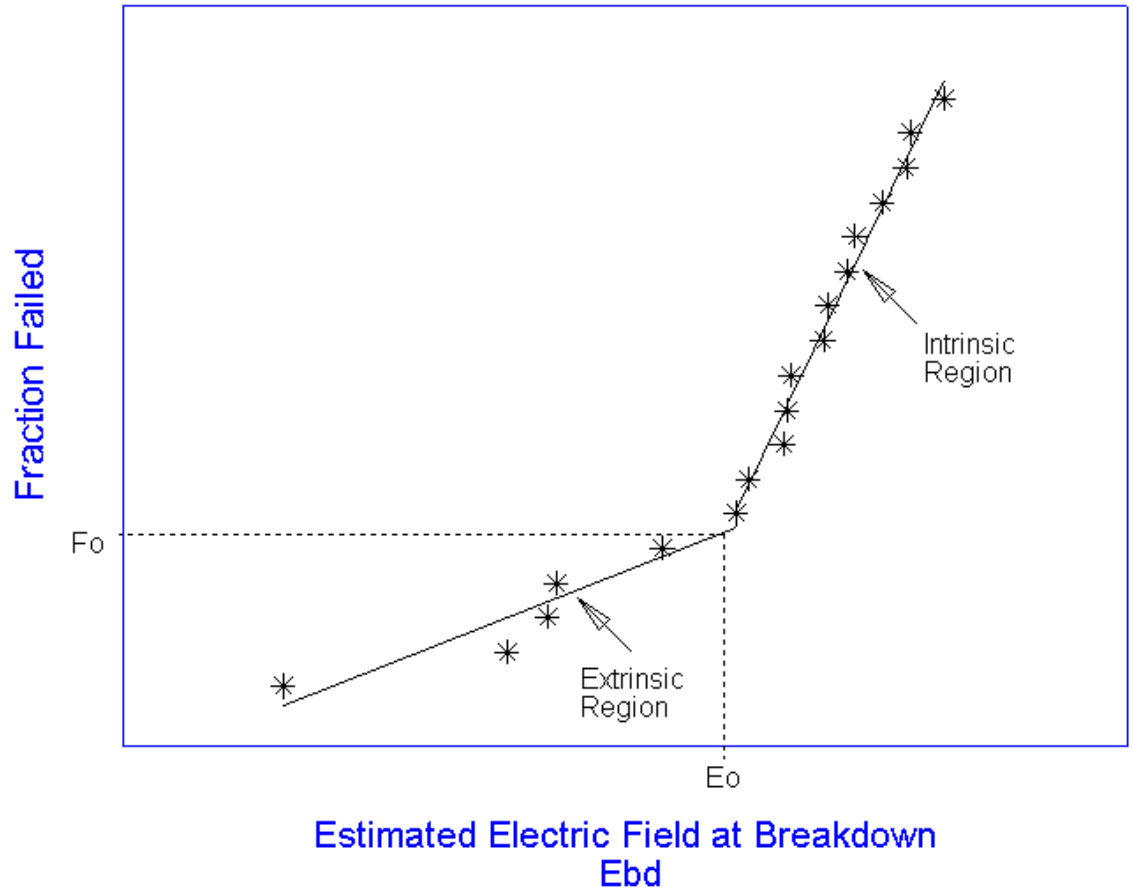


Figure A.1 — Cumulative breakdown distribution versus estimated electric field at breakdown. E_o is the estimated breakdown electric field that separates the intrinsic from the extrinsic distribution. F_o is the fraction defective.

The analysis of the breakdown charge density data is very similar to the analysis of the voltage breakdown data. The principal difference is that the breakdown charge density is plotted on a logarithmic scale, as illustrated in Figure A.2. This scale is necessary because the breakdown charge density typically ranges over several orders of magnitude. The vertical axis still has a normal probability scale as before. Usually, the resultant distribution is bimodal, as shown in Figure A.2 and can be interpreted in terms of an intrinsic and an extrinsic population. The same techniques as before [1] can be used to separate the distributions for these two populations. Typical values of breakdown charge density range from 0.1 to 10 C/cm^2.

Annex A Supplemental data analysis (cont'd)

A.2 Data analysis (cont'd)

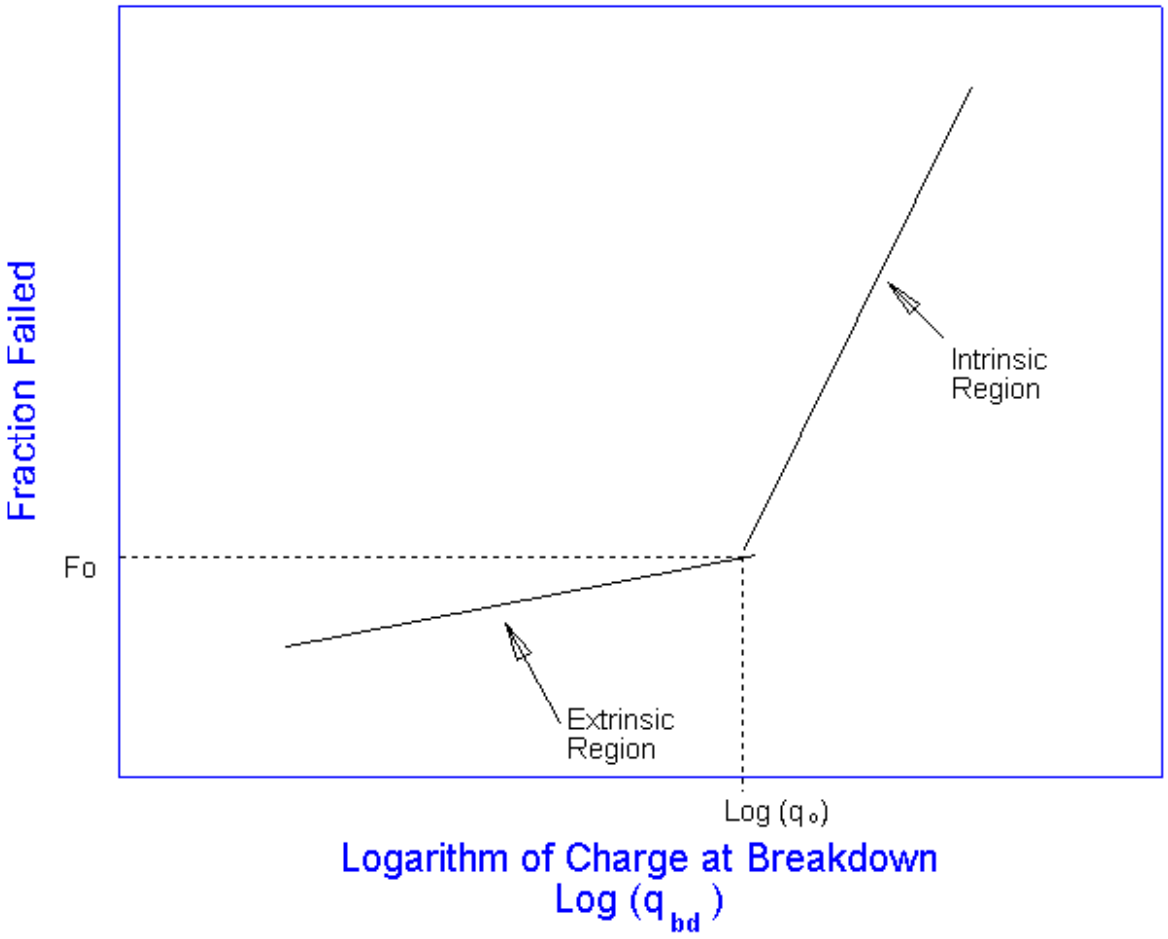


Figure A.2 — Cumulative breakdown distribution versus the logarithm of the charge density at breakdown. q_o is the charge density at breakdown that separates the intrinsic from the extrinsic distribution. F_o is the fraction defective.

Three parameters are of significant interest in analyzing these plots: the median and the standard deviation of the intrinsic population, and the percent of the population that is defective. The parameters pertaining to the intrinsic population are readily obtained after it is separated from the extrinsic population, as described in the previous sections. The percent defective is given by F_0 in Figure A.1. Notice that F_0 is not a direct measure of defect density because F_0 depends on the size of the test structure, as discussed further in Annex B. On the other hand, the intrinsic distribution is independent of test structure size. This property can be used to verify that a particular population is intrinsic, simply by testing capacitors of different sizes.

Annex A Supplemental data analysis (cont'd)

A.2 Data analysis (cont'd)

The ideal plot of breakdown data (estimated breakdown electric field or breakdown charge density) should have no extrinsic population (no "defective" oxides), a very small main population standard deviation (nearly a vertical line) and a very large median. This set of conditions implies that there would be no weak oxides to fail early, and that the intrinsic oxides would not fail until well beyond the intended device life. The most effective way to use this data is for continuously driving the distribution closer to its ideal shape by instituting appropriate process controls. A secondary use is for determining the oxide defect density, although the extremely large quantity of test data required to measure typical defect densities often makes this impracticable.

Data output from the wafer level oxide testing discussed in this procedure has many potential uses. The most beneficial use of this data in the manufacturing environment is for process control and reliability trend assessment. By using the results and analysis of these tests in a tight loop process improvement system, the manufacturer can continually monitor and improve the reliability of the product. In addition to serving as a monitor function, it is intended that these tests be inserted into a manufacturer's overall process nodes through extensive design of experiments' activities. Reliability trend assessment may be accomplished using standard Statistical Process Control procedures [2,3].

Because q_{bd} depends on area, design, ramp rate, step size and reading frequency, it should only be used as a process control monitor, not for determining relative oxide quality for different structures and/or measurement techniques. Any comparisons should be performed using Bounded J-Ramp on the identically designed structure with the same oxide thickness.

Naturally, decreasing the step size and increasing the measurement frequency can increase measurement accuracy.

A.3 Defect source analysis

While monitoring a process using the analysis techniques described in A.2 can ensure that a process is remaining under control, more sophisticated techniques are available to guide the user to the source of defects so that they may be reduced and ultimately eliminated. There are three steps to eliminating defects: 1) detecting the defect, 2) identifying the source of the defect, and 3) preventing the defect from occurring in the future. Annex C discusses in detail types of structures and the sizes needed to detect various levels of defects [1]. Techniques for identifying the source of defects [2] are discussed below. Methods of process modification to prevent defects from occurring [3] are numerous and complex, and are beyond the scope of this procedure.

Possible clues to the origin of oxide defects include the shape and location of the q_{bd} or V_{bd} histograms, the IV curves of individual oxides, failure analysis work on good and ruptured oxides, and comparative analysis of test data from different structures. Perhaps one of the easiest and most powerful techniques is this last one.

Annex A Supplemental data analysis (cont'd)

A.3 Defect source analysis (cont'd)

By designing a variety of structures, each that emphasizes a region in which defects can occur, the relative rate of defect occurrence in the various structures can indicate the region in which failure is occurring. Consider a case where three structures are used such that one emphasizes thin oxide area, one emphasizes poly over thin oxide edge, and one emphasizes the edge between field and thin oxide edge. A defect density may be estimated for the thin oxide area, D_a, the linear polysilicon to thin oxide edge, D_p, and the linear field oxide to thin oxide edge, D_f, by the simultaneous solution of three equations:

$$D_1 = N_1 (A_1 D_a + L_{p1} D_p + L_{f1} D_f) \quad \text{(A1)}$$

$$D_2 = N_2 (A_2 D_a + L_{p2} D_p + L_{f2} D_f) \quad \text{(A2)}$$

$$D_3 = N_3 (A_3 D_a + L_{p3} D_p + L_{f3} D_f) \quad \text{(A3)}$$

where: D_1, D_2, and D_3 (#) are the numbers of oxides with a defect from each of the three respective test structures found from data plotted as in Figures A1 and A2

N_1, N_2, and N_3 (#) are the respective numbers of parts tested from each of the three different structure types

A_1, A_2, and A_3 (cm^2) are the respective thin oxide areas of the three test structures used

L_{p1}, L_{p2}, and L_{p3} (cm) are the respective polysilicon to thin oxide edge lengths

L_{f1}, L_{f2}, and L_{f3} (cm) are the respective field oxide to thin oxide edge lengths

D_a (defects/cm^2) is the area defect density

D_p (defects/cm) is the linear defect density of the polysilicon over thin oxide edge

D_f (defects/cm) is the linear defect density of the field oxide and thin oxide edge.

This technique is most effective when a large quantity of parts is tested, gross defect problems exist, or the structures evaluated are extremely large. Otherwise, the left sides of the simultaneous equations presented above may become quite small, so that very few failures resulting from oxide defects may be observed. Defect density estimates obtained using this technique should only be used as relative quantities rather than as absolute numbers. Annex B discusses valid techniques for arriving at a statistically sound measurement of defect density.

Annex B Supplemental sampling plan statistics

B.1 Overview

This annex is not a formal part of the test procedures but is included for purposes of information.

Typical semiconductor production process defect densities are today at levels so low as to be extremely difficult to measure with any degree of precision. Consequently, the primary use of wafer level test structures is in qualitative applications, such as verification of process control or identification of defect sources, rather than as an absolute measure of defect density. However, in certain special applications it may be desirable to extract a statistically valid defect density.

This annex presents a three-step procedure that allows a manufacturer to: 1) determine the maximum defect density that must be demonstrated to ensure that no oxide defects exist on a production die (see B.2), 2) establish a sampling plan that allows a desired defect density of D_o or less to be demonstrated (see B.3), and 3) estimate defect density given a specific test result (see B.4 and B.5). Examples of how this procedure might be implemented are given in B.6.

Care must be taken when using these procedures to ensure that the sampling plans obtained are practical. In some cases, the total oxide area that must be sampled to prove the desired defect density level is prohibitively large, and the manufacturer should revert to statistical process control techniques rather than direct defect density measurement.

The intent of sampling plan procedures is twofold: 1) to allow a manufacturer to show that no defective oxides exist on production circuits, and 2) to allow tracking of defect density when a problem exists so that it may be effectively reduced. This is based on the premise that the best technique for managing the reliability implications of defect densities is to eliminate them. More sophisticated (and controversial) techniques are available that attempt to analyze defects and predict operating life failures resulting from those defects.

Two classes of defects can be identified: 1) those whose occurrence is distributed over the entire area of thin oxide, and 2) those whose occurrence is restricted, by their nature, to specific thin oxide edges. An example of the former is a random particle defect, while an example of the latter is a defect induced by white ribbon thinning. Defect densities can be calculated, monitored, and controlled for each of these types of defects independently. The three most common procedures for controlling this are to monitor the bulk oxide defects lumped together, the gate to source/drain edge effects lumped together, and the gate to field edge effects lumped together. (See Annex B3.)

The following procedure describes a technique to control bulk oxide defects, with B.5 describing a modification to this procedure that can be used to monitor both types of edge defects.

Annex B Supplemental sampling plan statistics (cont'd)

B.2 Determining an acceptable defect density level

Given a circuit with a total gate oxide area of A_c, the probability of finding one or more defects on that circuit is determined by the defect density of the process used to build that circuit. The defect density that results in a probability of 0.95 that no defects are present may be thought of as the defect density that assures, with 95% confidence, that no defective oxides are present. This defect density is called D_o, and is given by the equation:

$$D_o = \frac{-\ln(0.95)}{A_c} = \frac{0.0513}{A_c} \qquad \text{(B.1)}$$

where: A_c = Total gate area of circuit (cm^2)

D_o = Defect density to be proven (defects/cm^2).

Figure B.1 shows the D_o required for circuits with gate areas ranging from 0.00001 to 1 cm^2 to assure defect-free circuits. The lines on Figure B.1 show D_o confidence levels for 60%, 90%, 95%, 99%, and 99.9%

Equation B.1 is based on 0.95 probability of no defects occurring on a circuit, given a Poisson defect distribution. Calculations may be made based on other probability levels using the general equation relating defect density (D_o) to circuit area (A_c) and probability (C) of no failures:

$$D_o = \frac{-\ln(C)}{A_c} \qquad \text{(B.2)}$$

Annex B Supplemental sampling plan statistics (cont'd)

B.2 Determining an acceptable defect density level (cont'd)

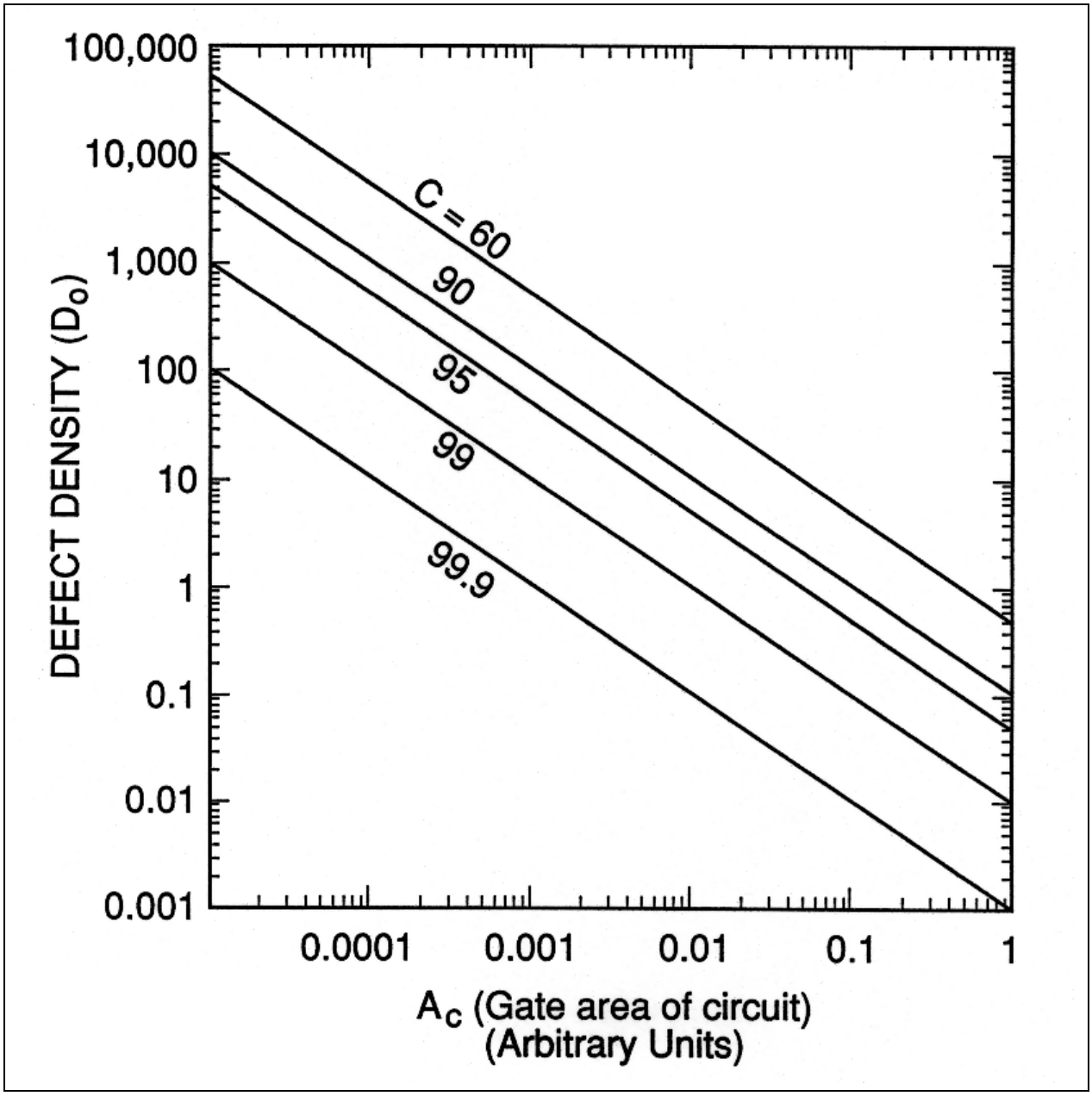


Figure B.1 — D_o required to assure that a circuit with total gate area A_c is defect free with confidence levels from 60 to 99.9 %.

Annex B Supplemental sampling plan statistics (cont'd)

B.3 Sampling required to demonstrate defect densities

This section describes statistical procedures for determining a sampling plan for demonstrating a given defect density. Consider the following:

D_o = Acceptable defect density (defects/cm^2)

A_t = Gate area of each test structure (cm^2)

N = Number of test structures sampled

A defect density of D_o or better can be proven by stressing N test structures, each of gate area A_t, and experiencing zero defect related failures. See Annex B for a description of "defect related failure."

Two procedures are described: one that allows determination of N if A_t is fixed, and one that allows determination of A_t if there are constraints on N.

B.3.1 Finding N given A_t

Equation B3 gives the relationship between sample size required and test structure area:

$$N \geq \frac{-\ln(1-0.95)}{A_t D_o} \qquad \text{(B.3)}$$

Figure B.2 illustrates this relationship for seven distinct values of D_o, ranging from 1000 defects/cm^2 to 0.001 defect/cm^2.

B.3.2 Finding A_t given N

Equation B4 gives the relationship between test structure area required and sample size:

$$A_t \geq \frac{-\ln(1-0.95)}{N D_o} \qquad \text{(B.4)}$$

Figure B.2 illustrates this relationship for seven distinct values of D_o, ranging from 1000 defects/cm^2 to 0.001 defect/cm^2.

Annex B Supplemental sampling plan statistics (cont'd)

B.3.2 Finding A_t given N (cont'd)

Equations B.3 and B.4 prove to a 95% confidence level (C) that the actual defect density is less than or equal to D_o, with no defective oxides allowed in a sample of size N. Equations B.3 and B.4 are specific solutions of the general equation:

$$C \le 1 - \sum_{i=Y}^{N} \frac{N!}{i!\,(N-i)!} \left[\exp(-D_o A_t)\right]^i \left[1 - \exp(-D_o A_t)\right]^{N-i} \qquad \text{(B.5)}$$

where: Y is the minimum acceptable number of non-defective oxides found among the N oxides tested.

NOTE — In Equations B.3 and B.4 that all oxides must be non-defective, so Y=N.

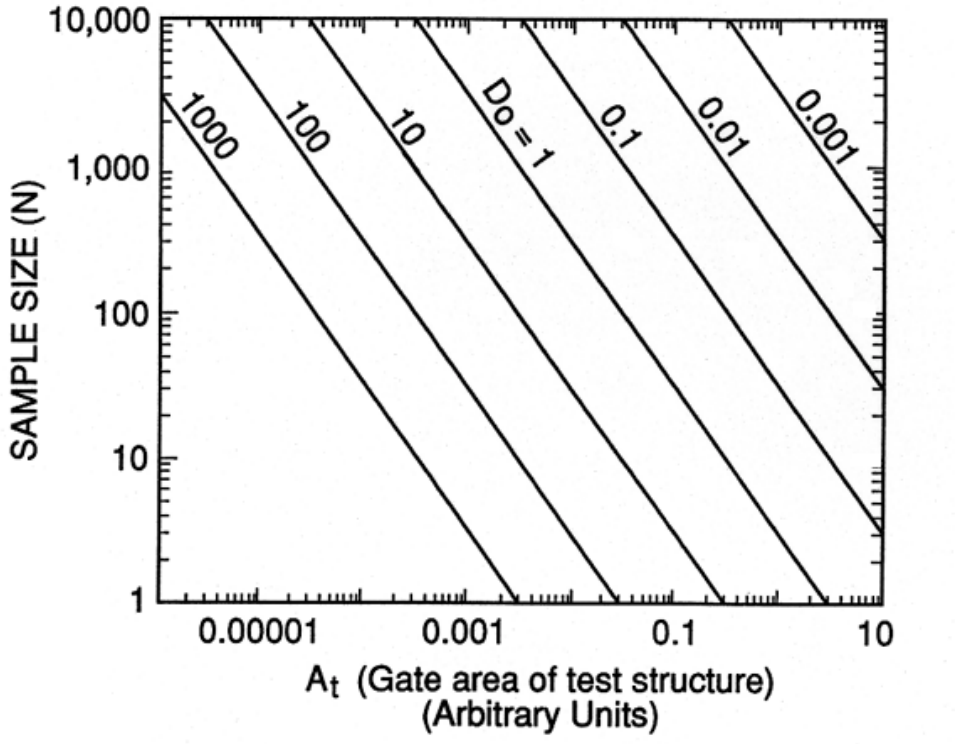


Figure B.2 — The sample size (N) versus the gate area of the test structure, for D_o ranging from 1000 cm^{-2} to 0.001 cm^{-2}.

Annex B Supplemental sampling plan statistics (cont'd)

B.4 Determining defect density from a test result

B.4 assumes a 95% confidence level that the defect density is D_o or better and uses Equation B.5 to generate Figure B.3.

Figure B.3 may be used to determine a best estimate of defect density given a sample size, N, the number of defective oxides found (curves for 0, 1, 2, 5, 10, and 50 defective oxides are shown), and a test structure with thin oxide area A_t. The vertical axis of the graph is the product of the estimated defect density, D_o, and the test structure thin oxide area, A_t.

To use Figure B3, find the sample size tested on the horizontal axis. Move up to the curve that represents the number of defective oxides found. If there is not a curve for the number found, perform a logarithmic interpolation between the two closest curves. Then, move to the left of the chart and read the value on the vertical axis. Divide this number by the area of the test structure to determine the estimate of defect density.

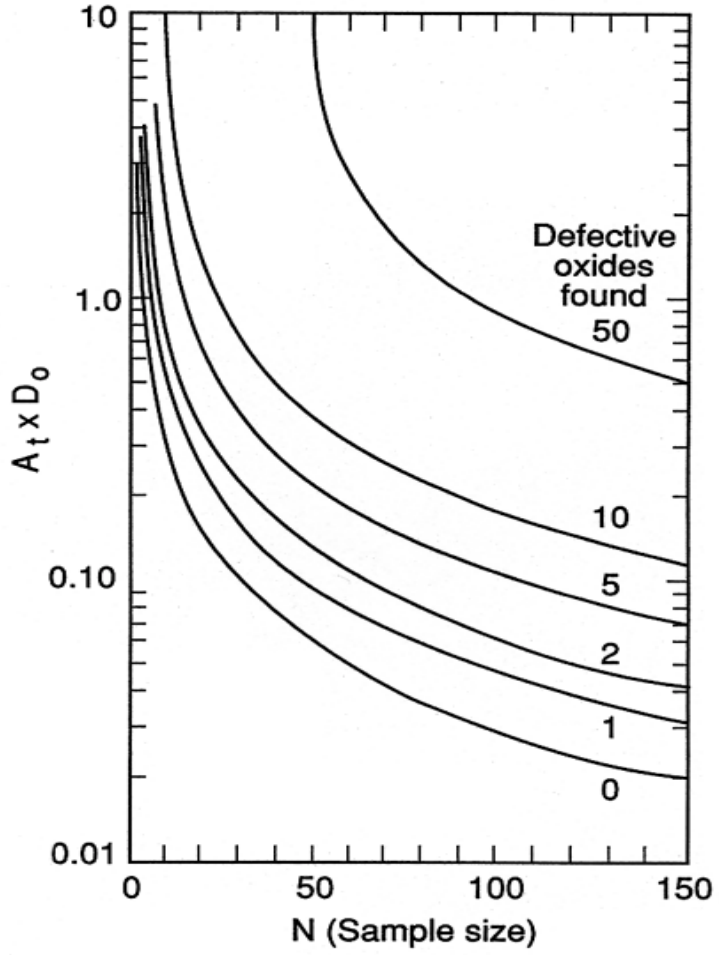


Figure B.3 — Best estimate of the defect density D_o, given a sample size N, the number of defective oxides found, and the area of the thin-oxide test structure A_t.

Annex B Supplemental sampling plan statistics (cont'd)

B.5 Ensuring acceptable edge defect densities

To ensure that an acceptable defect level is maintained for each of the oxide edges associated with a thin oxide (gate/drain, gate/field, plus others on more exotic devices), the same set of equations may be used if two minor changes are made:

1) In each instance in which an area is called for, a length is substituted. For example, rather than using A_c for the total area of the circuit, L_c would be used and would be a measure of, for example, the total gate to field oxide edge length of a circuit. Note that the units of measurement will be in cm rather than cm^2.

2) In each instance in which a defect density is called for, a defect per unit length value is substituted. This would have the dimensions of defects/cm rather than defects/cm^2.

All calculations, strategies, procedures, and plots remain identical with that described in this annex. Note that with this type of calculation, as well as with those in the remainder of this annex, only those defective oxides associated with the defect density to be measured should be considered. For example, when attempting to establish a defect density for polysilicon edge over thin oxide, only those structures that actually fail at that edge should be included. Other failures should be eliminated from the sample and replaced with an additional test structure. Failure analysis may sometimes be required to verify the defect location. Also, these procedures will not support the use of combined data from more than one test structure type as in Annex B.3.

B.6 Examples for use of defect density curves

B.6.1 and B.6.2 give two examples of how a manufacturer can design a test plan using a minimum sample size and how to estimate defect density.

B.6.1 Example 1 — Designing a test plan

A manufacturer desires to have a 95% confidence level that each die shipped contains no defective oxides. Each die has a total active thin capacitor area of 0.23 cm^2. A test structure is available with an area of 0.013 cm^2. It is desired that the minimum number of structures be tested.

B.6.1.1 Determining required maximum defect density

The first step is to use Figure B.1 to determine the defect density needed to provide the desired guarantee. Note that the units of the horizontal axis are not labeled. This is intentional, as any desired units can be used. Be aware, however, that defect density must from then on be calculated and expressed in terms of those same units. Consequently, by using an area measurement in square centimeters, it is necessary to use units of defects per square centimeter for all defect density terms.

B.6.1 Example 1 — Designing a test plan (cont'd)

B.6.1.1 Determining required maximum defect density (cont'd)

Figure B.4 shows how Figure B.1 would be used. First, find the circuit area on the horizontal axis. Then, move vertically until intersecting the line for 95% confidence. Proceed to the vertical axis directly to the left of the intersection point and read off the value of defect density listed there. This is the defect density needed to satisfy the manufacturer's requirements. In this case, the value read from the figure is approximately 0.2 defects/cm^2.

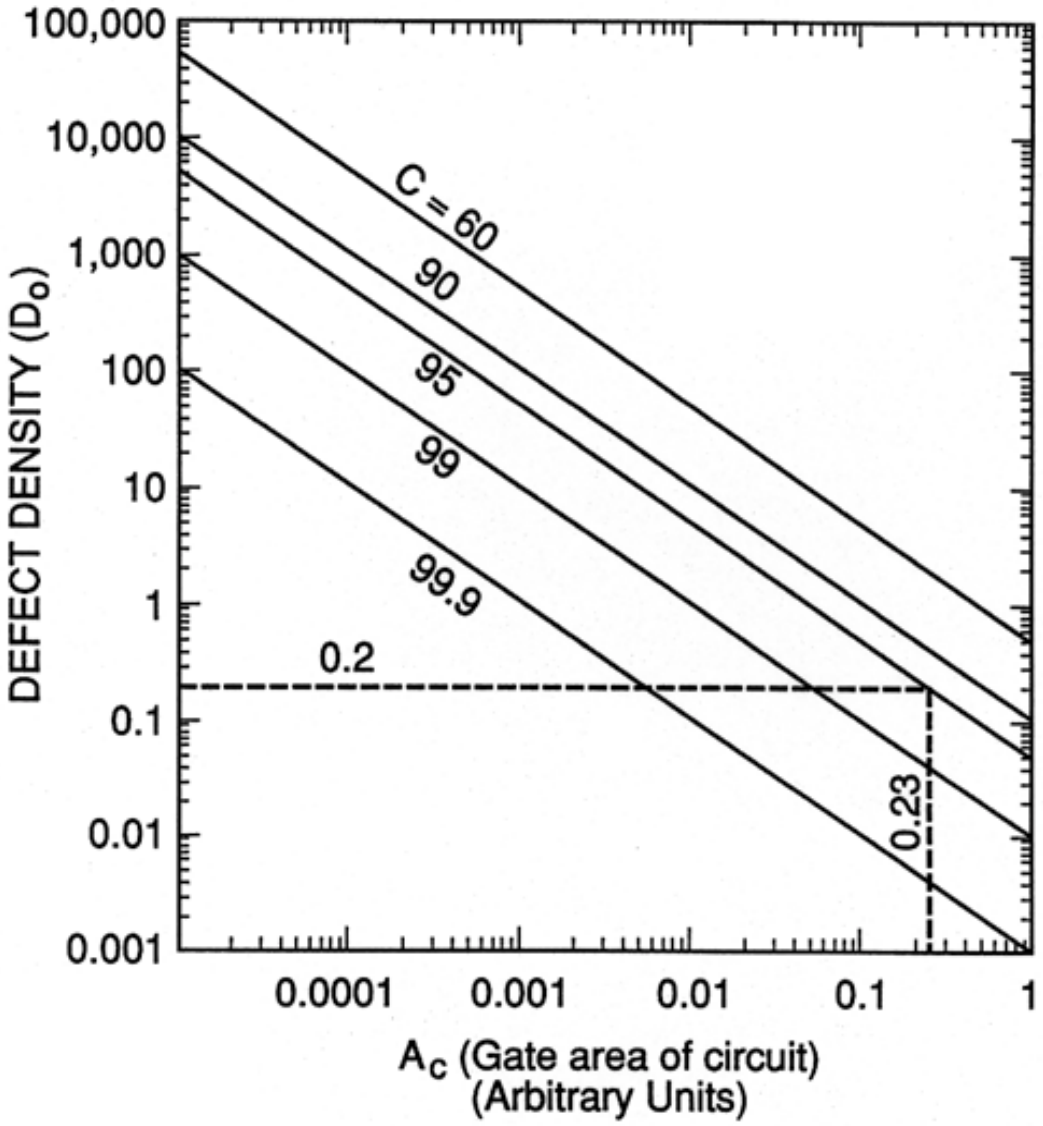


Figure B.4 — Illustration of how Figure B.1 is used to determine the defect density needed to provide the desired guarantee. (See B.6.1.1)

B.6.1 Example 1 — Designing a test plan (cont'd)

B.6.1.2 Establishing a sample plan

In order to minimize the sample size required to prove a defect density of 0.2 defect/cm^2, a test should be developed that is passed only when no failures occur from among the sampled population. Allowing failures would require a larger sample size to prove the same defect density. With no failures allowed, Figure B.2 may be used to determine the necessary sample size as shown in Figure B.5. First, find the area of the available test structure, 0.013 on the horizontal axis. Then, move vertically until the appropriate defect density line is intersected. In this case, the required defect density is 0.2 defect/cm^2, a value that is not explicitly plotted. Therefore, a "0.2 defect/cm^2" line will need to be interpolated between lines 0.1 and 1.0. Note that this should be a logarithmic interpolation. Following to the left from the intersection of this interpolated line gives a sample size of approximately 1000. Therefore, to make the desired claim using this test structure, 1000 structures must be tested and found to be defect free.

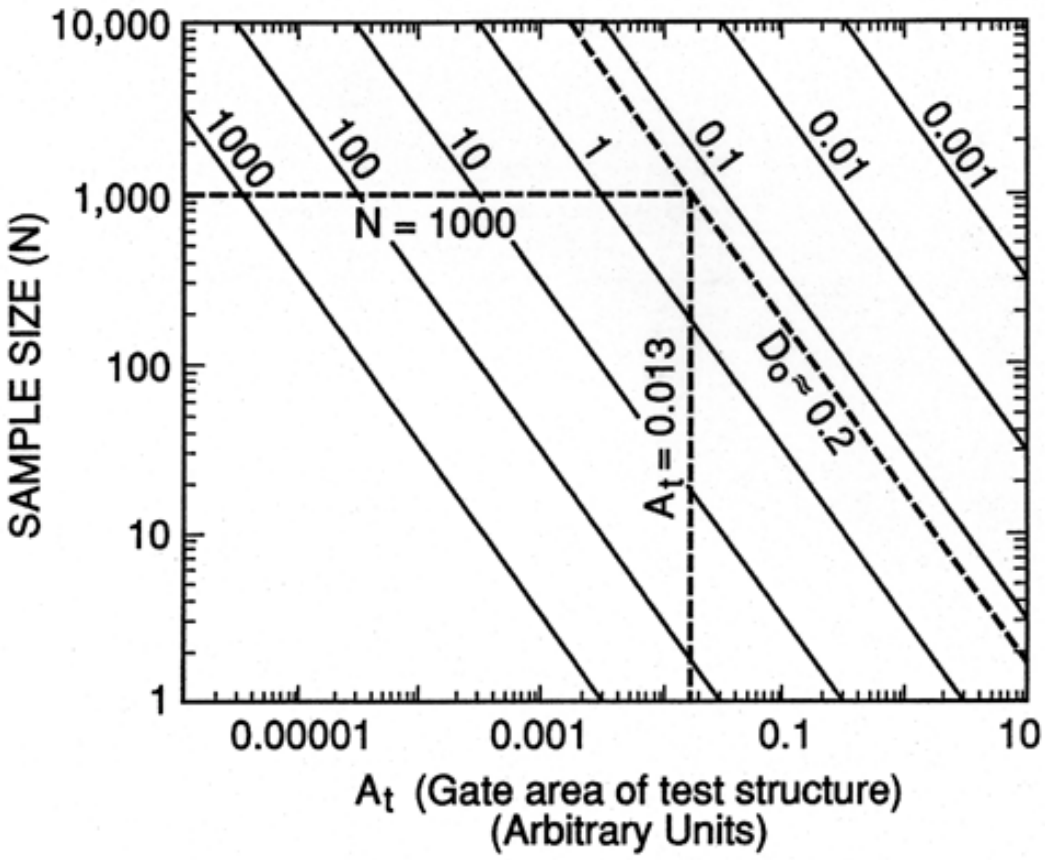


Figure B.5 — Illustration of how Figure B.2 is used to determine the sample size N, given the area of the test structure A_t, and the defect density D_o. (See B.6.1.2)

B.6.1 Example 1 — Designing a test plan (cont'd)

B.6.1.3 Reducing the required sample size

If the 1000 samples required in the above example is an unacceptably large sample size, several alternatives are available: 1) select a larger test structure, 2) provide a lower confidence level in your guarantee (e.g., 90% instead of 95%), or 3) use a smaller die with less total oxide area.

Note that in this example, a total test structure area of 1000 times 0.013 cm^2 was required to demonstrate a defect free oxide area of 0.23 cm^2. In other words, the ratio of area tested to area used was greater than 50. Although this number can vary greatly with confidence level and actual circuit area, it is not uncommon to have such a high ratio. This makes such a practice impracticable in a typical production environment.

B.6.2 Example 2 — Estimating defect density

Note that in the previous example, no information concerning defect density is obtained other than whether it is above or below the desired defect density. In order to estimate defect density, Figure B.3 is useful. Suppose a plan is implemented using a sample size of 65 test structures of area 0.1 cm^2 and one defective oxide is found. Figure B.6 demonstrates how Figure B.3 can be used to show that this will ensure a defect density of approximately 0.73 defect/cm^2. This is obtained in the following manner:

1) Find the sample size (65) on the horizontal axis.
2) Move vertically until the "1 failure" line is intersected.
3) Then move left to the vertical axis and read the "A_tD_o product." In this case, the product is 0.073.
4) To calculate defect density, simply divide the "A_tD_o product" by the test structure area, A_t. Since the test structure area here is 0.1, the defect density that has been demonstrated is 0.73 defect/cm^2 (0.073/0.1).

If a number of failures other than one are found, then simply repeat the above procedure, except move across to the vertical axis when the appropriate "failure" line is reached. For example, no defective oxides would indicate an "A_tD_o product" of 0.045, or a defect density of 0.45 defect/cm^2. Finding two defective oxides would indicate an "A_tD_o product" of 0.1, or a defect density of 1.0 defects/cm^2. Again, if a failure line does not exist for the situation experienced, a logarithmic interpolation should be used.

B.6 Examples for use of defect density curves (cont'd)

B.6.2 Example 2 — Estimating defect density (cont'd)

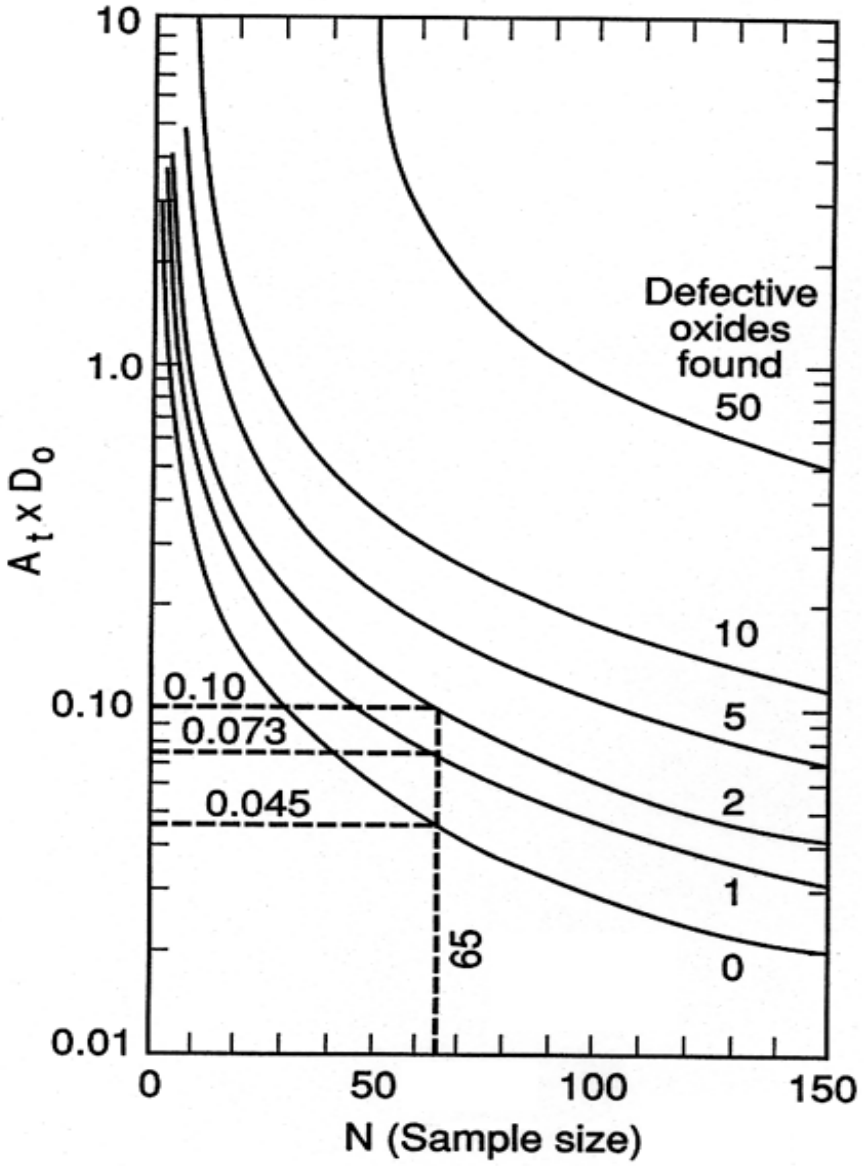


Figure B6 — Illustration of how Figure B3 is used to obtain the defect density D_o, given the sample size N, the number of failures, and the area of the thin oxide, A_t. (See section B6.2)

Annex C Fowler-Nordheim Tunneling Current

C.1 Fowler-Nordheim

This annex is not a formal part of the test procedures but is included for purposes of information.

In an ideal oxide having a thickness greater than 5nm, the current density, J, should fit the Fowler-Nordheim equation:

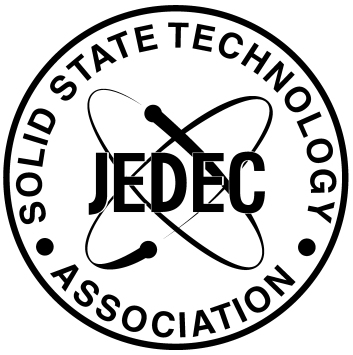
$$J = A \ E^2 \exp\left(-\frac{B}{E}\right) \qquad (5)$$

where A and B are constants related to the Si/SiO2 electron effective mass and the barrier height, as determined from a gate current versus field measurement. Typical values are in the order of:

$A = 1.6 \ \ MA / (MV)^2$

$B = 222 \ \ MV / cm$

Large deviations in the current density from the Fowler-Nordheim equation may indicate defective oxides.


SOLID STATE TECHNOLOGY
JEDEC
ASSOCIATION